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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHOE, HENRY	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,464	NILSON, CHRIS	
	Examiner	Art Unit	
	Henry K. Choe	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7,10,12-15 and 17-23* is/are rejected.

7)☒ Claim(s) *4,5,8,9,11 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, 7, 10, 12-15 and 17-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Winslow (Figs. 1-3).

Regarding claim 1, Winslow (Figs. 1-3) discloses an amplifier circuit comprising a first transistor (142 in Fig. 2), a biasing circuit [(150, CONTROL CIRCUIT); It should be noted that the elements 150 and CONTROL CIRCUIT can be read as the claimed biasing circuit since the elements 150 and CONTROL CIRCUIT affect the bias voltage of the transistor 142] including a process compensation circuit (150) and wherein the biasing circuit (150, CONTROL CIRCUIT) being coupled to a gate (gate of transistor 142) of the first transistor [(142); see column 4, lines 9-12].

Regarding claim 2, the process compensation circuit (150) includes a replica device circuit [(152 in Fig. 3); see column 4, lines 59-61].

Regarding claim 3, the replica device circuit (152 in Fig. 3) includes a replica transistor (152 in Fig. 3) that replicates the characteristics of the first transistor [(142); see column 4, lines 59-61].

Regarding claim 6, the process compensation circuit (150) and the first transistor (142) are included in a single integrated circuit (see column 2, lines 26-32).

Regarding claim 7, the biasing circuit (150, CONTROL CIRCUIT) further includes a bias control circuit (CONTROL CIRCUIT) coupled to the gate (gate of transistor 142) of the first transistor (142).

Regarding claim 10, the biasing circuit (150, CONTROL CIRCUIT) further includes a temperature compensation circuit (150) coupled to the gate (gate of transistor 142) of the first transistor (142). [It should be noted that the temperature compensation circuit (150) is coupled to the gate of the first transistor (142) through the resistors R4, R5 and operational amplifier 172. The term "coupled" is an open ended limitation which does not exclude any intervening elements. It should be noted that the claim does not recite that the temperature compensation circuit is directly coupled to the gate of the first transistor.]

Regarding claim 12, the temperature compensation circuit (150) and the first transistor (142) are included in a single integrated circuit (see column 2, lines 26-32).

Regarding claim 13, the amplifier circuit (Fig. 2 of Winslow) is included within a transmitter (see column 3, line 44).

Regarding claim 14, amplifier circuit (Fig. 2 of Winslow) is included within wireless data link transmitter (see column 3, line 13; It said, a device 13 is a mobile cellular telephone which indicates it is wireless).

Regarding claim 15, Winslow (Figs. 2 and 3) discloses an amplifier circuit comprising the method steps of producing (150) the process compensated DC bias voltage (+Vs, -Vs) in a process compensation circuit (150), and applying the process compensated DC bias voltage (+Vs, -Vs) to a gate (gate of transistor 142) of a first

transistor [(142); It should be noted that the process compensated DC bias voltage (+Vs, -Vs) is applying to a gate (gate of transistor 142) of the first transistor (142) through the resistors R4, R5 and operational amplifier 172. It should be also noted that the claim does not recite that directly applying the process compensated DC bias voltage to a gate of a first transistor], the process compensation circuit (150) and the first transistor (142) being on a single integrated circuit (see column 2, lines 26-32).

Regarding claim 17, adjusting (Vctl, Vreg) the process compensated DC bias voltage (+Vs, -Vs) to select (Vo) a desired class of operation for the first transistor [(142); It should be noted that the operating condition of the first transistor 142 depends on output voltage (Vo) of the operational amplifier 172.].

Regarding claim 18, adjusting (Vctl, Vreg) the process compensated DC bias voltage (+Vs, -Vs) includes receiving a control signal (Vctl).

Regarding claim 19, the control signal (Vctl) includes a digital control signal [prior to converting the control signal (Vctl) from the digital signal to the analog signal, the control signal (Vctl) was the digital signal.].

Regarding claim 20, the control signal (Vctl) can include converting the digital control signal to an analog signal (see column 5, lines 28-30).

Regarding claim 21, adjusting (Vctl, Vreg) the process compensated DC bias voltage (+Vs, -Vs) to compensated for a temperature of the integrated circuit (see column 4, lines 36-38).

Regarding claim 22, Winslow (Figs. 1-3) discloses an amplifier circuit comprising a first transmitter (19 in Fig. 1) including an amplifier (Fig. 2) which includes a first

transistor (142), a biasing circuit [(150, CONTROL CIRCUIT); It should be noted that the elements 150 and CONTROL CIRCUIT can be read as the claimed biasing circuit since the elements 150 and CONTROL CIRCUIT affect the bias voltage of the transistor 142] including a process compensation circuit (150) and wherein the biasing circuit (150, CONTROL CIRCUIT) being coupled to a gate (gate of transistor 142) of the first transistor [(142); see column 4, lines 9-12] and wherein the process compensation circuit (150) and the first transistor (142) are included in a single integrated circuit (see column 2, lines 26-32).

Regarding claim 23, Winslow (Figs. 1-3) discloses an amplifier circuit comprising a first transistor (142), a biasing circuit [(150, CONTROL CIRCUIT); It should be noted that the elements 150 and CONTROL CIRCUIT can be read as the claimed biasing circuit since the elements 150 and CONTROL CIRCUIT affect the bias voltage of the transistor 142] including a process compensation circuit (150) and wherein the biasing circuit (150, CONTROL CIRCUIT) being coupled to a gate (gate of transistor 142) of the first transistor [(142); see column 4, lines 9-12], and the biasing circuit (150, CONTROL CIRCUIT) including a process compensation circuit (150), a bias control circuit (CONTROL CIRCUIT) coupled to the gate (gate of transistor 142) of the first transistor (142), and a temperature compensation circuit (150) coupled to the gate (gate of transistor 142) of the first transistor (142) [It should be noted that the temperature compensation circuit (150) is coupled to the gate of the first transistor (142) through the resistors R4, R5 and operational amplifier 172. The term "coupled" is an open ended limitation which does not exclude any intervening elements. It should be noted that the

claim does not recite that the temperature compensation circuit is directly coupled to the gate of the first transistor.], and wherein the process compensation circuit (150) and the temperature compensation circuit (150) and the first transistor (142) are included in a single integrated circuit (see column 2, lines 26-32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seymour et al (Fig. 4).

Seymour et al (Fig. 4) discloses an amplifier circuit comprising a first transistor (104'), and a biasing circuit (102') including a process compensation circuit [(D1, C3); see column 3, lines 17-19] and the biasing circuit (102') being coupled to a base (base of 104') of the first transistor (104'). As described above, Seymour et al (Fig. 4) discloses all the limitations in the claim 1 except for that the first transistor being a Field Effect Transistor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted well known art-recognized equivalent transistors such as a Field Effect Transistor in place of the bipolar transistor in the circuit

of the Seymour et al (Fig. 4) because such a modification would have been considered a mere substitution of art-recognized equivalent transistor.

Allowable Subject Matter

Claims 4, 5, 8, 9, 11 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

HENRY CHOE
PRIMARY EXAMINER

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